EE/CprE/SE 491 WEEKLY REPORT 03

2/16/2020 – 3/1/2020

Group number: 08

Project title: High Resolution Digitally Trimmable Resistor

Client &/Advisor: Prof. Randy Geiger

Team Members/Role: Clark Reimers - Test Engineer, Pierce Nablo - Design Engineer, Alek Benson - Information Manager, Oluwatosin Oyenekan - Meeting Lead

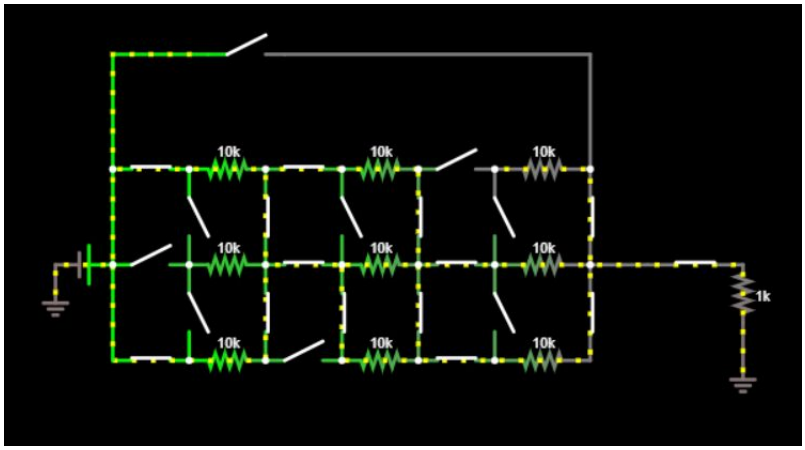
❖ Weekly Summary

During the past 2 weeks, the group started to shift focus from researching existing trimmable resistor designs to generating unique ideas. Then, the group made a presentation and presented new ideas to Dr. Geiger. Also the group attempted to make a couple schematics of the current trimmable resistor structures. This will give an initial performance to compare other designs to. Also, the team worked on section one and two of the design document.

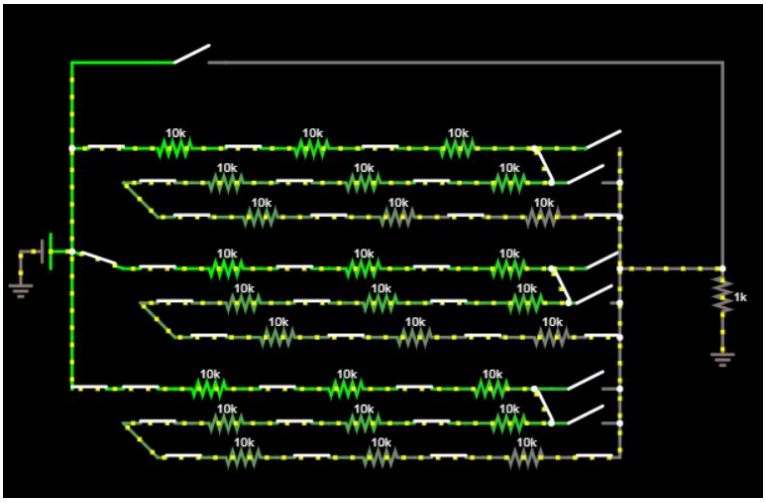
❖ Past week accomplishments

Clark Reimers:

- Researched various methods of trimming resistors.
    - Brainstormed ideas that incorporated these methods (see image below)



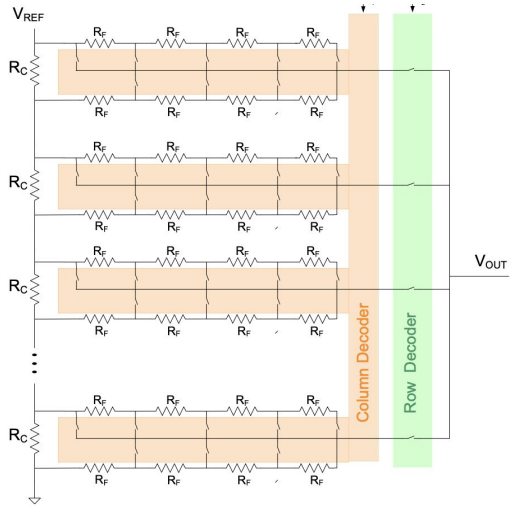
    - Improved upon these ideas (see image below)

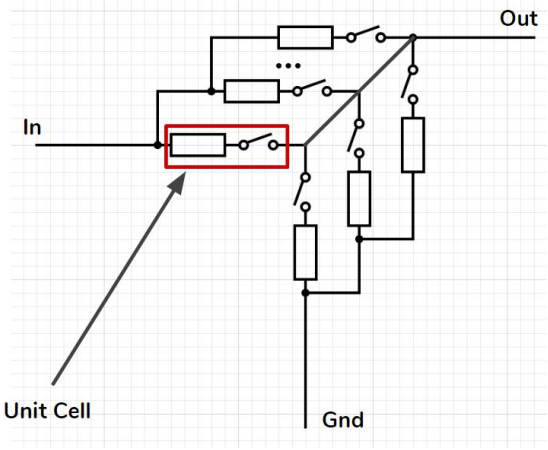


- Started testing some basic design
- Troubleshooted tech issues
- Contributions to weekly assignments
- Presented some designs to Dr.Geiger and the group to expand upon them.

Pierce Nablo:

- Brainstormed a few circuit designs that are influenced by DAC structures

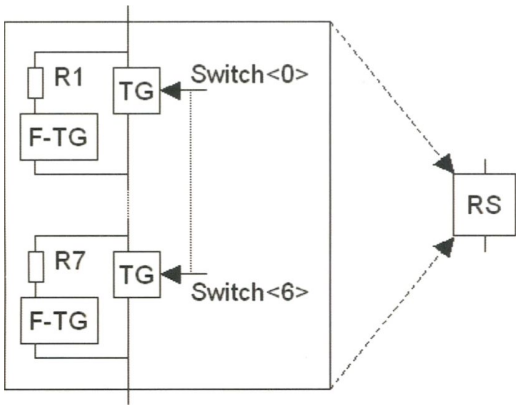




- Presented to Dr. Geiger on the few circuit ideas that created
- Made schematics in Virtuoso for the basic structures
    - Series design
    - Parallel design
    - Matrix design
- Completed weekly assignments for EE491

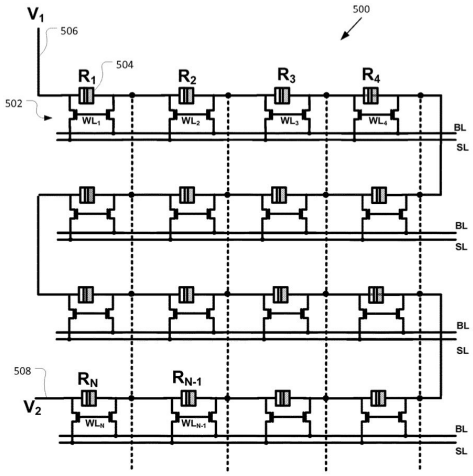
Alek Benson:

- Researched some more resistor structures
    - Methods using dummy transistors- create a similar TC
- Researched some TC solutions
    - Using Negative Temperature Coefficient circuit components
- Learned about DAC designs with Dr. Geiger's 435 slides
- Contributed to our weekly meeting slides and presented some findings to the group.



Oluwatosin Oyenekan:

- Researched deeper on Trimming resistors, and some methods we could use
    - Did some calculation using these method
- Presented to Dr Geiger and the team my findings
- Organized our weekly meetings.
- Completed weekly assignments for EE491



❖ **Pending issues**

Clark Reimers:

- No pending issues.

Pierce Nablo:

- Virtuoso would not run on a remote desktop session.

Alek Benson:

- No issues

Oluwatosin Oyenekan

- No issue faced

❖ **Individual contributions**

Name	**Hours this period**	**Hours cumulative**
Clark Reimers	15	39
Pierce Nablo	15	39
Alek Benson	12	35
Oluwatosin Oyenekan	12	36

❖ **Plans for the upcoming week**

Clark Reimers: continue to do research and continue to brainstorm new ideas that can be used in application of the overall circuit. The next step will be to continue testing this circuit as it progresses. The next milestone is to finalize a few of the brainstormed designs and to simulate them along with the reference designs for comparisons.

Alek Benson: The plan is to keep learning from Geiger's 435 slides, come up with some designs using negative temperature coefficients, and then simulate a design in Virtuoso.

Oluwatosin Oyenekan: come up with new ideas for the circuit and simulate them along with ideas already found out , organize meetings with the advisor. My goal for this period is to test out and get a positive result from at least one circuit.

Pierce Nablo: Continue trying to get Virtuoso to run on a remote session. Make new circuit designs that could mitigate temperature effects. Get a simulation of the reference series circuit design.

- **Summary of weekly advisor meeting**

  The meeting was held in our weekly scheduled meeting room in Coover and was productive. We clarified our direction for research and found a good basis of reference designs and some potential designs to start simulating. We improved on our potential designs and found a few promising methods to address our project constraints.